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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/849,799	HENRY ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *May 26, 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30, 34-39, 45-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30, 34-39, 45-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Hazm. Fleming

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/10/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/15/04,7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: IDS-9/13/05, 9/28/05, 10/20/05, 5/26/06, and 4/25/06 (11 IDS pages considered in total).

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 51-70 and 72-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 73 is dependent on claim 32. Since claim 32 has been cancelled, the dependency of claim 73 on claim 32 is improper. For the purposes of examination, claim 73 is interpreted to be dependent on claim 28 instead. Appropriate correction is required.

4. In claim 51, the limitation "if the first target address prediction does not match the second target address..." is unclear. Examiner is unable to discern the metes and bounds of the claim. It appears that Applicant is attempting to claim the mere possibility that limitations might be in the claims based on alternate claim language. It is unclear whether the limitation "if the first target address prediction does not match the second target address..." and limitations following must actually be present in the claims. When the first target address prediction matches the second target address, then nothing after the limitation has to be present according to the claim. Therefore, for the purposes of examination, limitations including and after the "if" limitation are ignored since they appear to not necessarily be required according to claim 51. Applicant should claim active and definite limitations, such that it is clear what must be present in the claim for a reference to read on the claim.

5. Furthermore, claims 52-70 and 72-77 contain similar unclear alternate claim limitations of claim 51. Therefore, for the purposes of examining claims 52-70 and 72-77, limitations after or related to "if" or "only if" are ignored since they appear to not necessarily be required according to the claims *(Alternate claim limitations not required to be found in the prior art are printed in an italic font below for Applicant's convenience.).*

6. Additionally, even if the alternate limitations were read into the claims 51, 56, 61 and 66, the alternate limitations are unclear. It appears that applicant has attempted to claim the invention similar to the manner in which a programmer would write pseudo code, but has omitted any hierarchical order of operations syntax. For example, in claim 51 the "if" in line 13 is immediately followed by an indented "if" in line 15, with the limitation "overriding..." beginning at line 17. Do both "if" statements in lines 13 and 15 need to be met for the "overriding" limitation at line 17 to follow? Or does only the "if" at line 15 need to be met for the "overriding" limitation to follow? The spacing of the limitations of the claims lead the Examiner to believe that Applicant intended to mean that both "if" statements in lines 13 and 15 need to be met for the "overriding" limitation at line 17 to follow, however it's not completely clear. The same problem appears with the "if" limitation at line 20 and the "foregoing" limitation at line 22. Do all "if" statements in lines 13, 15 and 20 need to be met for the "foregoing" limitation at line 22 to follow? Or does the "if" at lines 15 and 20 need to be met, or only the "if" at line 20? The spacing of the limitations of the claims lead the Examiner to believe that Applicant intended to mean that both "if" statements in lines 13 and 20 need to be met for the "foregoing" limitation at line 22 to follow, however it's not clear as presently claimed. Similar problems occur in claim 56, the "if" statements at lines 8, 11, 13 and 18, claim 61, the "if"

statements at lines 24, 26 and 32, and claim 66, lines 12, 14, 16 and 22. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. Claims 1, 2, 15-30, 34-39, 45, 48, 50 and 71-73 are rejected under 35 U.S.C. 102(b) as being anticipated by Emma et al., US Patent 5,353,421 (hereinafter "Emma").

8. Referring to claim 1, Emma et al. have taught a branch prediction apparatus in a processor including address selection logic for providing a fetch address to an instruction cache, the fetch address used to select lines of the instruction cache, the apparatus comprising:

a. first and second branch predictors, for providing first and second target address predictions of a branch instruction to the address selection logic (abstract, Figure 10, elements 12 and 55, column 4, lines 1-44);

b. instruction decode logic, configured to receive and decode said branch instruction and to generate a type thereof (abstract, Figure 10, element 17); and

c. branch control logic, configured to control the address selection logic to select said first prediction as the fetch address, said first prediction selecting a first line of the instruction cache (Figure 10, abstract, column 4, lines 1-44, column 7, lines 3- 12);

d. wherein said branch control logic is further configured to subsequently selectively control the address selection logic, based on said branch instruction type, to select said second prediction as the fetch address, said second prediction selecting a second line of the instruction cache (Figure 10, abstract, column 4, lines 1-44, column 5, lines 35-68, column 17, lines 25-55).

9. Referring to claim 2, Emma et al. have taught the apparatus of claim 1, as described above, and further comprising:

a. comparison logic, coupled to said first and second branch predictors, for comparing said first and second target address predictions (Figure 10, abstract, column 17, lines 39-45, column 9, lines 20-65).

10. Referring to claim 15, Emma et al. have taught the apparatus of claim 2, as described above, and wherein said first and second predictors are also configured to provide said first and second target address predictions of a conditional branch instruction to the address selection logic, wherein said type includes a specification of whether said branch instruction is a conditional type branch instruction (column 11, lines 18-58).

11. Referring to claim 16, Emma et al. have taught the apparatus of claim 15, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a conditional branch instruction and said first and second predictions miscompare (column 11, lines 18-58, column 13, line 65-column 14, line 14).

12. Referring to claim 17, Emma et al. have taught the apparatus of claim 15, as described above, and wherein said first and second predictors provide first and second direction predictions of said conditional branch instruction to said branch control logic for predicting whether said conditional branch instruction will be taken (column 11, line 66-column 12, line 30).

13. Referring to claim 18, Emma et al. have taught the apparatus of claim 17, as described above, and further comprising:

a. second comparison logic, coupled to said first and second branch predictors, for comparing said first and second direction predictions of said conditional branch instruction (Figure 10, abstract, column 17, lines 3 9-45, column 9, lines 20-65).

14. Referring to claim 19, Emma et al. have taught the apparatus of claim 18, wherein said branch control logic controls the address selection logic to select an instruction pointer of a next sequential instruction to said conditional branch instruction as the fetch address if said second direction prediction predicts said conditional branch instruction will not be taken (column 12, lines 16-30).

15. Referring to claim 20, Emma et al. have taught the apparatus of claim 19, as described above, and wherein said branch control logic controls the address selection logic to select said next sequential instruction pointer if said second direction prediction predicts said conditional branch instruction will not be taken and said first and second direction predictions miscompare (column 12, lines 16-30).

16. Referring to claim 21, Emma et al. have taught the apparatus of claim 2, as described above, and wherein said branch control logic subsequently selectively controls the address selection logic based on said branch instruction type to select said second prediction as the fetch address if said first and second predictions do not match (Figure 10, abstract, column 4, lines 1-44, column 5, lines 35-68, column 17, lines 25-55).

17. Referring to claim 22, Emma et al. have taught the apparatus of claim 1, as described above. Emma et al. have not specifically taught wherein said branch instruction type comprises an Intel IA-32 instruction set branch instruction type. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the branch instructions

of Emma et al. be implemented as any type of branch instruction, including and Intel IA-32 instruction set branch instruction, for the desirable purpose implementing and benefiting from this invention in a widely used instruction set.

18. Referring to claim 23, Emma et al. have taught the apparatus of claim 1, as described above, and wherein said first branch predictor receives the instruction cache fetch address and provides said first target address prediction in response to the fetch address (abstract, Figure 10, column 7, lines 3-32).

19. Referring to claim 24, Emma et al. have taught the apparatus of claim 23, as described above, and wherein said first branch predictor provides said first target address prediction in response to the fetch address whether or not a branch instruction is present in a third line of the instruction cache, said third instruction cache line selected subsequent to selection of said first instruction cache line (abstract, column 17, lines 39-55).

20. Referring to claim 25, Emma et al. have taught the apparatus of claim 23, as described above, and wherein said first branch predictor provides said first target address prediction prior to said instruction decode logic decoding said branch instruction (abstract, column 4, line 1-44).

21. Referring to claim 26, Emma et al. have taught the apparatus of claim 1, as described above, and wherein said first branch predictor comprises a branch target address cache indexed by the instruction cache fetch address (column 7, line 54-column 8, line 22).

22. 18. Referring to claim 27, Emma et al. have taught the apparatus of claim 1, as described above, and wherein said first branch predictor comprises a speculative call return stack (column 8, lines 23-55).

23. Claims 28, 29 30, 34, 35, 36, 39, and 45 do not recite limitations above the claimed invention set forth in claims 1 and 2 and are therefore rejected for the same reasons set forth in the rejection of claims 1 and 2 above.

24. Referring to claim 71, Emma has taught the apparatus of claim 28, as described above, and further comprising:

a. wherein said first branch predictor is further configured to provide a first direction prediction of said branch instruction, prior to said instruction decode logic decoding said branch instruction and generating said type thereof, said first direction prediction for predicting whether said branch instruction will be taken or not taken (Figure 10, abstract, column 4, lines 1-44, column 7, lines 3-12, BHT, branch history table); and

b. a branch history table for providing a second direction prediction based on said type of said branch instruction, said second direction prediction for predicting whether said branch instruction will be taken or not taken (Figure 10, abstract, column 4, lines 1-44, column 5, lines 35-68, column 17, lines 25-55, DHT, decode history table).

25. Referring to claim 72, Emma has taught the apparatus of claim 28, wherein *if said branch type is a conditional branch type, said comparison logic compares first and second direction predictions, respectively. (Alternate claim limitation not required to be found in the prior art.)*

26. Referring to claim 73, Emma has taught the apparatus of claim 32 (Assumed to be dependent on claim 28), wherein *if said first and second direction predictions do not match, said control logic overrides said first prediction with said second prediction. (Alternate claim limitation not required to be found in the prior art.)*

27. Referring to claim 37, Emma et al. have taught the processor of claim 36, as described above, and further comprising:

a. an instruction cache, coupled to an address bus for receiving a fetch address, said fetch address selecting a line of instructions for provision to said instruction decode logic (Figure 10, elements 13, 11, 16, an 17).

28. Referring to claim 38, Emma et al. have taught the processor of claim 37, as described above, and wherein said speculative branch predictor makes said speculative prediction even though a possibility exists that no branch instruction is present in said line of instructions (column 7, line 53-2column 8, line 22, A prediction is always made for each instruction. A miss in the BHT predicts the next sequential instruction.).

29. Claim 48 does not recite limitations above the claimed invention set forth in claims 1,2, 15, and 16 and is therefore rejected for the same reasons set forth in the rejection of claim 1,2, and 15, and 16 above.

30. Claim 50 does not recite limitations above the claimed invention set forth in claims 1,2, 15, 17, 18, and 19 and is therefore rejected for the same reasons set forth in the rejection of claims 1, 2, 15, 17, 18, and 19 above.

31. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

32. Claims 51-70 and 74-77 are rejected under 35 U.S.C. 102(e) as being anticipated by McCormick, Jr. et al., US Patent 6,351,796 (hereinafter "McCormick").

33. Referring to claim 51, McCormick has taught a method for processing a branch instruction in a pipelined microprocessor having an instruction cache, the method comprising:

a. fetching a cache line containing the branch instruction from the instruction cache (column 6, lines 6-10, column 8, lines 50-63, column 9, lines 47-57);

b. generating a first prediction of a target address of the branch instruction concurrently with said fetching (column 9, lines 47-57, column 12, lines 17-21, column 4, lines 21, speculative prediction at the front end);

c. branching instruction fetching to the first target address prediction (column 4, lines 6-21);

d. determining a type of the branch instruction, after said branching to the first target address prediction, wherein the type is one of a plurality of predetermined branch instruction types (column 12, lines 10-34, column 6, line 5-column 12, line 35, column 16, lines 50-56);

e. generating a second prediction of the target address of the branch instruction based on the type of the branch instruction, after said determining the type of the branch instruction (column 16, lines 50-56, column 17, line 65-column 18, line 9, non-speculative prediction at the back end); and

f. *if the first target address prediction does not match the second target address prediction:*

if the type of the branch instruction is a first of the plurality of predetermined types:

overriding said branching to the first target address prediction by branching instruction fetching to the second target address prediction; and

if the type of the branch instruction is a second of the plurality of predetermined types: foregoing overriding said branching to the first target address prediction. (Alternate claim limitations not required to be found in the prior art.)

34. Referring to claim 52, McCormick has taught the method as recited in claim 51, wherein *the second of the plurality of predetermined types is an indirect branch instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 51.).*

35. Referring to claim 53, McCormick has taught the method as recited in claim 51, wherein *the first of the plurality of predetermined types is a program counter-relative branch instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 51.).*

36. Referring to claim 54, McCormick has taught the method as recited in claim 51, wherein *the first of the plurality of predetermined types is a return branch instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 51.).*

37. Referring to claim 55, McCormick has taught the method as recited in claim 51, wherein *the first of the plurality of predetermined types is a conditional branch instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 51.).*

38. Referring to claim 56, McCormick has taught the method as recited in claim 55, further comprising:

a. generating a first prediction of a direction of the branch instruction (column 4, lines 6-21, taken/not taken), *wherein said branching instruction fetching to the first target address prediction is performed only if the first direction prediction predicted the branch instruction will be taken (Alternate claim limitation not required to be found in the prior art.);*

b. generating a second prediction of the direction of the branch instruction, after said determining the type of the branch instruction (column 16, lines 50-56, column 17, line 65-column 18, line 9, column 4, lines 6-21, non-speculative prediction at the back end); and

c. *if the type of the branch instruction is the conditional branch instruction type: determining whether the first direction prediction matches the second direction prediction; and if the first direction prediction does not match the second direction prediction: if the second direction prediction predicted the branch instruction will be taken: overriding said branching to the first target address prediction by branching instruction fetching to the second target address prediction; and if the second direction prediction predicted the branch instruction will not be taken: overriding said branching to the first target address prediction by branching instruction fetching to a next*

instruction sequential to the branch instruction. (Alternate claim limitations not required to be found in the prior art.)

39. Referring to claim 57, McCormick has taught the method as recited in claim 51, wherein said generating a first prediction of a target address of the branch instruction is performed without knowing whether the branch instruction is actually present in the cache line (column 9, lines 46-57, column 10, lines 40-column 12, lines 35).

40. Referring to claim 58, McCormick has taught the method as recited in claim 51, further comprising:

a. storing a history of target addresses of previously executed branch instructions, prior to said fetching a cache line containing the branch instruction (column 4, lines 42-56, column 8, lines 50-63), *wherein said generating the first prediction of the target address is performed only if the history contains a target address for the branch instruction; and branching instruction fetching to the second target address prediction, if the history does not contain a target address for the branch instruction. (Alternate claim limitations not required to be found in the prior art.)*

41. Referring to claim 59, McCormick has taught the method as recited in claim 58, further comprising: *generating a prediction of a direction of the branch instruction, if the type of the branch instruction is a conditional branch instruction type; and said branching instruction fetching to the second target address prediction, only if the direction prediction predicted the branch instruction will be taken. (Alternate claim limitations not required to be found in the prior art.)*

42. Referring to claim 60, McCormick has taught the method as recited in claim 51, further comprising:

a. executing the branch instruction to determine a correct target address of the branch instruction, after said branching to the second target address prediction, wherein the correct target address is not a prediction (column 4, lines 22-44); *and branching instruction fetching to the correct target address, if the second target address does not match the correct target address. (Alternate claim limitation not required to be found in the prior art.)*

43. Referring to claim 61, McCormick has taught a pipelined microprocessor having an instruction cache, comprising:

a. instruction fetch logic, configured to fetch a first cache line containing a branch instruction from the instruction cache (column 6, lines 6-10, column 8, lines 50-63, column 9, lines 47-57);

b. a first branch predictor, coupled to said instruction fetch logic, configured to generate a first prediction of a target address of the branch instruction concurrently with fetching the first cache line (column 9, lines 47-57, column 12, lines 17-21, column 4, lines 21, speculative prediction at the front end);

c. wherein said instruction fetch logic is configured to fetch a second cache line from the instruction cache at the first target address prediction after fetching the first cache line (column 4, lines 6-21);

d. instruction decode logic, coupled to said instruction fetch logic, configured to determine a type of the branch instruction after the first branch predictor generates the

first prediction, wherein the type is one of a plurality of predetermined branch instruction types (column 12, lines 10-34, column 6, line 5-column 12, line 35, column 16, lines 50-56);

e. *a second branch predictor, coupled to said instruction decode logic, configured to generate a second prediction of the target address of the branch instruction if the type of the branch instruction is a first of the plurality of predetermined types (Alternate claim limitation not required to be found in the prior art.);*

f. a third branch predictor, coupled to said instruction decode logic, configured to generate the second prediction of the target address of the branch instruction if the type of the branch instruction is a second of the plurality of predetermined types; (Alternate claim limitation not required to be found in the prior art.) and

g. comparison logic, coupled to said instruction fetch logic, for comparing the first and second target address predictions (column 18, lines 40-49);

h. *wherein if the first target address prediction does not match the second target address prediction: if the type of the branch instruction is the first of the plurality of predetermined types: said instruction fetch logic is configured to override the first branch predictor by fetching a third cache line from the instruction cache at the second target address prediction; and whereas if the type of the branch instruction is the second of the plurality of predetermined types: said instruction fetch logic is configured to forego overriding the first branch predictor. (Alternate claim limitations not required to be found in the prior art.)*

44. Referring to claim 62, McCormick has taught the microprocessor as recited in claim 61, *wherein the second of the plurality of predetermined types is an indirect branch instruction type, wherein said third branch predictor comprises a branch predictor for predicting target addresses of indirect branch instructions (Alternate claim limitation not required to be found in the prior art.).*

45. Referring to claim 63, McCormick has taught the microprocessor as recited in claim 61, wherein *the first of the plurality of predetermined types is a program counter-relative branch instruction type, wherein said second branch predictor comprises a branch predictor for predicting target addresses of program counter-relative branch instructions (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 61.).*

46. Referring to claim 64, McCormick has taught the microprocessor as recited in claim 61, wherein *the first of the plurality of predetermined types is a return branch instruction type, wherein said second branch predictor comprises a branch predictor for predicting target addresses of return instructions (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 61.).*

47. Referring to claim 65, McCormick has taught the microprocessor as recited in claim 61, wherein *the first of the plurality of predetermined types is a conditional branch instruction type, wherein said second branch predictor comprises a branch predictor for predicting target addresses of conditional branch instructions (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 61.).*

48. Referring to claim 66, McCormick has taught the microprocessor as recited in claim 65, further comprising:

a. wherein said first branch predictor is further configured to generate a first prediction of a direction of the branch instruction (column 4, lines 6-21, taken/not taken), *wherein said instruction fetch logic fetches the second cache line from the instruction cache at the first target address prediction only if the first direction prediction predicted the branch instruction will be taken (Alternate claim limitation not required to be found in the prior art.);*

b. a fourth branch predictor, configured to generate a second prediction of the direction of the branch instruction, if the type of the branch instruction is the conditional branch instruction type (Alternate claim limitation not required to be found in the prior art.); and

c. second comparison logic, coupled to said instruction fetch logic, configured to compare the first and second direction predictions (column 18, lines 40-49);

d. *wherein if the type of the branch instruction is the conditional branch instruction type: if the first direction prediction does not match the second direction prediction: if the second direction prediction predicted the branch instruction will be taken: said instruction fetch logic is configured to override the first branch predictor by fetching a third cache line from the instruction cache at the second target address prediction; and whereas if the second direction prediction predicted the branch instruction will not be taken: said instruction fetch logic is configured to override the first branch predictor by fetching a third cache line from the instruction cache containing a next instruction sequential to the branch instruction (Alternate claim limitations not required to be found in the prior art.).*

49. Referring to claim 67, McCormick has taught the microprocessor as recited in claim 61, wherein said first branch predictor generates the first target address prediction without knowing whether the branch instruction is actually present in the first cache line (column 9, lines 46-57, column 10, lines 40-column 12, lines 35).

50. Referring to claim 68, McCormick has taught the microprocessor as recited in claim 61, wherein said first branch predictor comprises:

a. a branch target address cache (BTAC), configured to store a history of target addresses of previously executed branch instructions, prior to fetching the first cache line containing the branch instruction (column 4, lines 42-56, column 8, lines 50-63), *wherein said BTAC generates the first prediction of the target address only if the history contains a target address for the branch instruction (Alternate claim limitation not required to be found in the prior art.); and*

b. wherein said instruction fetch logic is configured to fetch the third cache line from the instruction cache at the second target address prediction, if the history does not contain a target address for the branch instruction (Alternate claim limitation not required to be found in the prior art.).

51. Referring to claim 69, McCormick has taught the microprocessor as recited in claim 68, *wherein said BTAC is further configured to generate a prediction of a direction of the branch instruction if the type of the branch instruction is a conditional branch instruction type, wherein said instruction fetch logic is configured to fetch the second cache line from the instruction cache at the second target address prediction, only if the direction prediction predicted the*

branch instruction will be taken (Alternate claim limitations not required to be found in the prior art.).

52. Referring to claim 70, McCormick has taught the microprocessor as recited in claim 61, further comprising:

a. an execution unit, coupled to said instruction fetch logic, configured to execute the branch instruction to determine a correct target address of the branch instruction, after said instruction fetch logic branches to the second target address prediction, wherein the correct target address is not a prediction (column 4, lines 22-44); and

b. *wherein said instruction fetch logic is further configured to fetch a fourth cache line from the instruction cache at the correct target address, if the second target address does not match the correct target address (Alternate claim limitation not required to be found in the prior art.).*

53. Referring to claim 74, McCormick has taught a pipelined processor, comprising:

a. a branch target address cache, for providing a speculative target address prediction of a branch instruction prior to decoding of said instruction (column 9, lines 47-57, column 12, lines 17-21, column 4, lines 21, speculative prediction at the front end);

b. a target address calculator, for calculating a non-speculative target address prediction of said branch instruction after said decoding of said branch instruction (column 16, lines 50-56, column 17, line 65-column 18, line 9, non-speculative prediction at the back end); and

c. a comparator, coupled to said branch target address cache and said target address calculator, for comparing said speculative and non-speculative target address predictions (column 18, lines 40-49);

d. wherein said processor branches to said speculative target address prediction (column 4, lines 6-21), *wherein the processor subsequently branches to said non-speculative target address prediction if said speculative and non-speculative target address predictions miscompare and if said instruction is a type comprised in a first set of instruction types. (Alternate claim limitations not required to be found in the prior art.)*

54. Referring to claim 75, McCormick has taught the processor of claim 74, wherein *said first set of instruction types includes a return instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 74.).*

55. Referring to claim 76, McCormick has taught the processor of claim 74, wherein *said first set of instruction types includes a program counter-relative branch instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 74.).*

56. Referring to claim 77, McCormick has taught the processor of claim 74, wherein *said first set of instruction types includes a conditional branch instruction type (Elements are a part of alternate claim limitations not required to be found in the prior art in claim 74.).*

Claim Rejections - 35 USC § 103

57. Claims 3-5 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emma et al., US Patent 5,353,421, in view of Gochman et al, US Patent 5,964,868 (hereinafter "Gochman").

58. Referring to claim 3, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not specifically taught wherein said type includes a specification of whether said branch instruction is a return type branch instruction. However Gochman et al. have taught wherein said type includes a specification of whether said branch instruction is a return type branch instruction (Gochman et al., Column 4, line 8-column 5, line 18, column 2, lines 17-28) for the desirable purpose of implementing the speculative return stack buffer so that instructions can continue to be fetched while a main memory access occurs. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of

59. Emma et al., include a specification of whether said branch instruction is return type branch instruction, as taught by Gochman et al., for the desirable purpose of being able to implement the speculative return stack buffer so that instructions can continue to be fetched while a main memory access occurs (Gochman et al., Column 4, line 8-column 5, line 18, column 2, lines 17-28).

60. Referring to claim 4, Emma et al. in combination with Gochman et al. have taught the apparatus of claim 3, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a return instruction and said first and second predictions miscompare (Gochman et al., column 7, lines 1-37, Emma et al., column 17, lines 13-5).

61. Referring to claim 5, Emma et al. in view of Gochman et al. have taught the apparatus of claim 4, as described above, and wherein said second branch predictor comprises a call return stack for providing said second target address prediction of said return instruction (Gochman et al., Column 4, line 8-column 5, line 18, column 2, lines 17-28).

62. Claim 47 does not recite limitations above the claimed invention set forth in claims 1-4 and is therefore rejected for the same reasons set forth in the rejection of claims 1-4 above.

63. Claims 6-14, 46, and 49 are rejected under 35 U.S .C. 103(a) as being unpatentable over Emma et al., US Patent 5,353,421, in view of Rappoport et al., US Patent 6,601,161 (hereinafter "Rappaport").

64. Referring to claim 6, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not specifically taught wherein said type includes a specification of whether said branch instruction is a program counter-relative type branch instruction. Rappoport et al. have taught said type includes a specification of whether said branch instruction is a program counter-relative type branch instruction (Rappoport et al., column 9, line 50-column 10, line 42, column 2, lines 1 - 12) so that the predictor that predicts indirect branches, or program counter-relative branches, most accurately is used. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of

65. Emma et al., include a specification if whether said instruction is a program counter-relative branch type instruction as taught by Rappoport et al. for the desirable purpose of using the predictor that most accurately predicts program counter-relative branches (Rappoport et al., column 9, line 50-column 10, line 42, column 2, lines 1-12).

66. Referring to claim 7, Emma et al. in combination with Rappoport et al. have taught the apparatus of claim 6, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a program counter-relative branch instruction and said first and second predictions miscompare (Rappoport et al., line 50-column 10, line 42).

67. Referring to claim 8, Emma et al. have taught the apparatus of claim 7, as described above, and wherein said second branch predictor comprises an arithmetic unit for calculating said second target address prediction based on an instruction pointer of said branch instruction (column 11, lines 1-17).

68. Referring to claim 9, Emma et al. have taught the apparatus of claim 8, as described above, and wherein said arithmetic unit calculates said second target address prediction using said instruction pointer of said branch instruction (column 11, lines 1-17).

69. Referring to claim 10, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not taught wherein said type includes a specification of whether said branch instruction is a direct type branch instruction. However, Rappoport et al. have taught wherein said type includes a specification of whether said branch instruction is a direct type branch instruction (Rappoport et al., column 9, line 10-column 10, line 66) for the desirable purpose of using the predictor that will most likely predict the direct branch correctly.

70. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of Emma et al, includes a specification of whether said branch instruction is a direct type branch instruction, as taught by Rappoport et al. for the desirable purpose of using the predictor that will most likely predict the direct branch correctly.

71. Referring to claim 11, Emma et al. have taught the apparatus of claim 10, as described above, and wherein said branch control logic controls the address selection logic to select said second target address prediction if said branch instruction type is a direct branch instruction and said first and second predictions miscompare (column 13, line 67-column 14, line 14).

72. Referring to claim 12, Emma et al. have taught the apparatus of claim 2, as described above. Emma et al. have not specifically taught wherein said type includes a specification of whether said branch instruction is an indirect type branch instruction. However, Rappoport et al. have taught wherein said type includes a specification of whether said branch instruction is an indirect type branch instruction (Rappoport et al., column 9, line 50-column 10, line 42) so that the predictor that predicts indirect branches most accurately is used. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the type of Emma et al., include a specification if whether said branch instruction is an indirect branch type instruction as taught by Rappoport et al. for the desirable purpose of using the predictor that most accurately predicts indirect branches (Rappoport et al., column 9, line 50-column 10, line 42).

73. Referring to claim 13, Emma et al. in view of Rappoport et al. have taught the apparatus of claim 12, as described above, and wherein said branch control logic controls the address selection logic not to select said second target address prediction if said branch instruction type is an indirect branch instruction (Rappoport et al., line 50-column 10, line 42).

74. Referring to claim 14, Emma et al. have taught the apparatus of claim 13, as described above, and wherein said second branch predictor comprises a branch target buffer for caching branch target addresses of previously executed indirect branch instructions (Rappoport et al., line 50-column 10, line 42).

75. Claim 46 does not recite limitations above the claimed invention set forth in claims 1, 2, 6, and 7 and is therefore rejected for the same reasons set forth in the rejection of claims 1, 2, 6, and 7 above.

76. Claim 49 does not recite limitations above the claimed invention set forth in claims 1,2, 12, 13, and 14 and is therefore rejected for the same reasons set forth in the rejection of claims 1, 2, 12, 13, and 14 above.

Response to Arguments

77. Applicant's arguments filed May 26, 2006 have been fully considered but they are not persuasive.

78. On pages 16 and 17, Applicant argues in essence:

> *"Neither Emma's DHT nor Hughes' branch predictor provides a target address of a branch instruction that has the possibility of being the incorrect target address of the branch instruction. Although Emma's DHT and Hughes' branch predictor provide an outcome prediction (taken/not taken) that has the possibility of being incorrect, Emma's address generate function and Hughes address formulation logic always generate the correct target address regardless of whether the direction prediction is correct or incorrect. Consequently, neither Emma's DHT not Hughe's branch predictor teach a branch predictor that provides a target address prediction, which is a limitation recited by claim 1."*

a. However, applicant has literally merely claimed "first and second branch predictors, for providing first and second target address predictions of a branch instruction to the address selection logic." The limitation "first and second target address predictions" is extremely vague. Any prediction, of or relating to a target address, reads on the limitation.

b. Emma has in fact taught "first and second branch predictors, for providing first and second target address predictions of a branch instruction to the address selection logic." when it is interpreted at least two different ways:

i. A first interpretation to apply Emma:

A predictor that produces a taken/not taken prediction is a prediction of whether a branch instruction will have a sequential target address or some other specified target address. One of these predicted target addresses is correct and the other predicted target address is incorrect. So one of Emma's predictors provides an address of a branch instruction that has the possibility of being incorrect. As such Emma has in fact taught "first and second branch predictors, for providing first and second target address predictions of a branch instruction to the address selection logic (Figure 10, elements 12 and 55, abstract, column 4, lines 1-44)." Therefore, this argument is moot.

ii. A second interpretation to apply Emma:

A complete branch target address prediction has two components, a target address and a direction (taken/not taken). When any one of the components of the prediction is incorrect, the entire prediction is incorrect. So when the direction is predicted to be incorrect, then the entire target address prediction is incorrect. So one of the branch target address predictions of Emma has the possibility of being incorrect. The target address prediction is incorrect when the direction is predicted incorrectly. As such Emma has in fact taught "first and second branch predictors, for providing first and second target address predictions of a branch instruction to the address selection logic (Figure 10, elements 12 and 55, abstract, column 4, lines 1-44)." Therefore this argument is moot.

c. If applicant would like specific limitations read into the claims, then applicant should specifically, distinctly and clearly claim those limitations. Again, the limitation

"first and second target address predictions" is extremely vague. Any prediction, of or relating to a target address, reads on the claim limitation. Therefore this argument is moot.

Conclusion

79. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

80. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

81. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday with first Friday's off.

82. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

83. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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